

## CLAIMS:

1. A flash-type analog-to-digital (A/D) converter, said A/D converter adapted to convert an input voltage  $V_{IN}$  to a digital output, wherein  $V_{IN}$  is within a working voltage range of the A/D converter, said working voltage range defined by a lowest voltage  $V_{REF-}$  and a highest voltage  $V_{REF+}$ , said A/D converter comprising:

$N$  reference voltages  $V_1, V_2, \dots, V_N$  non-linearly distributed between  $V_{REF-}$  and  $V_{REF+}$  and ordered according to  $V_{REF-} < V_1 < V_2 < \dots < V_N < V_{REF+}$ , wherein  $N$  is at least 3;  $N$  comparators associated with said  $N$  reference voltages on a one-to-one basis, each comparator adapted to make a comparison between  $V_{IN}$  and the reference voltage that is associated with said comparator, each comparator comprising bit-generating means for generating a binary bit that reflects a binary result of said comparison; and encoder means for generating the digital output from an analysis of the binary bits generated by said bit-generating means.

2. The A/D converter of claim 1, wherein the reference voltages  $V_1, V_2, \dots, V_{M-1}$  are linearly distributed between  $V_{REF-}$  and  $V_M$ , and wherein  $1 < M < N$ .

3. The A/D converter of claim 1, wherein the reference voltages  $V_1, V_2, \dots, V_{M-1}$  are linearly distributed between  $V_{REF-}$  and  $V_M$  with a constant reference voltage step size  $\Delta V_1$ , wherein the reference voltages  $V_{M+1}, \dots, V_N$  are linearly distributed between  $V_M$  and  $V_{REF+}$  with a constant reference voltage step size  $\Delta V_2$ , wherein  $\Delta V_1 < \Delta V_2$ , and wherein  $1 < M < N$ .

4. The A/D converter of claim 1, wherein the reference voltages  $V_1, V_2, \dots, V_{M-1}$  are linearly distributed between  $V_{REF-}$  and  $V_M$ , wherein the reference voltages  $V_{M+1}, \dots, V_N$  are geometrically distributed between  $V_M$  and  $V_{REF+}$ , and wherein  $1 < M < N$ .

5. The A/D converter of claim 1, wherein the reference voltages  $V_1, V_2, \dots, V_N$  are geometrically distributed between  $V_{REF-}$  and  $V_{REF+}$ .

6. The A/D converter of claim 1, wherein an error in the multibit string relative to  $V_{IN}$  (relative error) is a piecewise continuous function of  $V_{IN}$  the range of  $V_{REF-}$  to  $V_{REF+}$ .

$\pm V_{REF+}$ , said piecewise continuous function of  $V_{IN}$  having a plurality of pieces, wherein each two consecutive pieces of the plurality of pieces are discontinuously joined together, and wherein the relative error within each said piece is a monotonically decreasing function of  $V_{IN}$ .

7. The A/D converter of claim 6, wherein each piece of the plurality of pieces has about a same maximum relative error.

8. A method for converting an input voltage  $V_{IN}$  to a digital output such that  $V_{IN}$  falls between a lowest voltage  $V_{REF-}$  to a maximum voltage  $V_{REF+}$ , said method comprising: providing  $N$  reference voltages  $V_1, V_2, \dots, V_N$  non-linearly distributed between  $V_{REF-}$  and  $V_{REF+}$  and ordered according to  $V_{REF-} < V_1 < V_2 < \dots < V_N < V_{REF+}$ , wherein  $N$  is at least 3;;

comparing  $V_{IN}$  with each of the  $N$  reference voltages;

generating a binary bit for each said comparisons, said binary bit reflecting a binary result of said comparison; and

generating the digital output from an analysis of the generated binary bits.

9. The method of claim 8, wherein the reference voltages  $V_1, V_2, \dots, V_{M-1}$  are linearly distributed between  $V_{REF-}$  and  $V_M$ , and wherein  $1 < M < N$ .

10. The method of claim 8, wherein the reference voltages  $V_1, V_2, \dots, V_{M-1}$  are linearly distributed between  $V_{REF-}$  and  $V_M$  with a constant reference voltage step size  $\Delta V_1$ , wherein the reference voltages  $V_{M+1}, \dots, V_N$  are linearly distributed between  $V_M$  and  $V_{REF+}$  with a constant reference voltage step size  $\Delta V_2$ , wherein  $\Delta V_1 < \Delta V_2$ , and wherein  $1 < M < N$ .

11. The method of claim 8, wherein the reference voltages  $V_1, V_2, \dots, V_{M-1}$  are linearly distributed between  $V_{REF-}$  and  $V_M$ , wherein the reference voltages  $V_{M+1}, \dots, V_N$  are geometrically distributed between  $V_M$  and  $V_{REF+}$ , and wherein  $1 < M < N$ .

12. The method of claim 8, wherein the reference voltages  $V_1, V_2, \dots, V_N$  are geometrically distributed between  $V_{REF-}$  and  $V_{REF+}$ .
13. The method of claim 8, wherein an error in the multibit string relative to  $V_{IN}$  (relative error) is a piecewise continuous function of  $V_{IN}$  the range of  $V_{REF-} \leq V_{IN} \leq V_{REF+}$ , said piecewise continuous function of  $V_{IN}$  having a plurality of pieces, wherein each two consecutive pieces of the plurality of pieces are discontinuously joined together, and wherein the relative error within each said piece is a monotonically decreasing function of  $V_{IN}$ .
14. The method of claim 13, wherein each piece of the plurality of pieces has about a same maximum relative error.
15. A system for converting an input voltage  $V_{IN}$  to a digital output, comprising:  
 $K$  linear flash-type analog-to-digital (A/D) converter apparatuses  $Z_1, Z_2, \dots, Z_K$  respectively characterized by reference voltage step sizes  $\Delta V_1, \Delta V_2, \dots, \Delta V_K$  and respectively adapted to convert  $V_{IN}$  into multibit strings  $S_1, S_2, \dots, S_K$ , wherein  $\Delta V_1 < \Delta V_2 < \dots < \Delta V_K$ , and wherein  $K \geq 2$ ; and  
encoder means for combining  $S_1, S_2, \dots$ , and  $S_K$  to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within  $S_1, S_2, \dots$ , and  $S_K$ .
16. The system of claim 15, wherein  $S_1, S_2, \dots$ , and  $S_K$  each have a same number of bits.
17. The system of claim 15, wherein  $S_1, S_2, \dots$ , and  $S_K$  do not each have a same number of bits.
18. The system of claim 15, wherein for  $k=1, 2, \dots, K$  the A/D converter apparatus  $Z_k$  comprises an arithmetic unit  $A_k$  in series with an A/D converter  $B_k$ , wherein the A/D converters have a same working voltage range, wherein  $V_{IN}$  is within the working voltage range, wherein the working voltage range comprises  $K$  contiguous voltage subranges denoted as  $\delta V_1, \delta V_2, \dots, \delta V_K$  in order of lower to higher voltages, wherein for  $k=1, 2, \dots, K$  the arithmetic unit  $A_k$  is adapted to change  $V_{IN}$  into a new input voltage  $V_{IN,k}$  in

accordance with a transformation of  $\delta V_k$  into the working voltage range and A/D converter  $B_k$  is adapted to transform  $V_{IN,k}$  into the multibit string  $S_k$ .

19. The system of claim 18, wherein  $\delta V_1, \delta V_2, \dots, \delta V_K$  have values such the relative error of the digital output is a piecewise continuous function of  $V_{IN}$  within the working voltage range, said piecewise continuous function of  $V_{IN}$  having  $K$  pieces, wherein each two consecutive pieces of the  $K$  pieces are discontinuously joined together, wherein the relative error within each said piece of the  $K$  pieces is a monotonically decreasing function of  $V_{IN}$ , and wherein each piece of the  $K$  pieces has about a same maximum relative error.

20. The system of claim 15, wherein  $K=2$ , wherein the A/D converter apparatuses  $Z_1$  and  $Z_2$  comprise A/D converters  $B_1$  and  $B_2$  having working voltage ranges  $\delta_1$  and  $\delta_2$ , respectively, such that  $\delta_2$  is a subset of  $\delta_1$  and  $\delta_2/\delta_1$  is an integer subject to  $\delta_2/\delta_1 > 1$ , wherein  $B_1$  and  $B_2$  are respectively adapted to convert  $V_{IN}$  to  $S_1$  and  $S_2$ , and wherein the encoder means is adapted to generate the digital output as  $S_2$  if  $S_2$  is not within the voltage range  $\delta_1$  else the encoder means is adapted to generate the digital output as  $S_1$  multiplied by  $\delta_2/\delta_1$ .

21. The system of claim 20, wherein  $\delta_2/\delta_1 = 2^J$ , and wherein  $J$  is a positive integer.

22. A method for converting an input voltage  $V_{IN}$  to a digital output, comprising:  
 providing  $K$  linear flash-type analog-to-digital (A/D) converter apparatuses  $Z_1, Z_2, \dots, Z_K$  respectively characterized by reference voltage step sizes  $\Delta V_1, \Delta V_2, \dots, \Delta V_K$ , wherein  $\Delta V_1 < \Delta V_2 < \dots < \Delta V_K$ , and wherein  $K \geq 2$ ;  
 converting  $V_{IN}$ , by converter apparatuses  $Z_1, Z_2, \dots, Z_K$ , into multibit strings  $S_1, S_2, \dots, S_K$ , respectively; and  
 combining  $S_1, S_2, \dots, S_K$  to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within  $S_1, S_2, \dots, S_K$ .

23. The system of claim 22, wherein  $S_1, S_2, \dots, S_K$  each have a same number of bits.

24. The method of claim 22, wherein  $S_1$ ,  $S_2$ , ..., and  $S_K$  do not each have a same number of bits.

25. The method of claim 22, wherein for  $k=1, 2, \dots, K$  the A/D converter apparatus  $Z_k$  comprises an arithmetic unit  $A_k$  in series with an A/D converter  $B_k$ , wherein the A/D converters have a same working voltage range, wherein  $V_{IN}$  is within the working voltage range, wherein the working voltage range comprises  $K$  contiguous voltage subranges denoted as  $\delta V_1, \delta V_2, \dots, \delta V_K$  in order of lower to higher voltages, said method further comprising:

changing  $V_{IN}$  by the arithmetic unit  $A_k$  for  $k=1, 2, \dots, K$ , into a new input voltage  $V_{IN,k}$  in accordance with a transformation of  $\delta V_k$  into the working voltage range; and transforming  $V_{IN,k}$  by the A/D converter  $B_k$ , into the multibit string  $S_k$ .

26. The method of claim 25, wherein  $\delta V_1, \delta V_2, \dots, \delta V_K$  have values such the relative error of the digital output is a piecewise continuous function of  $V_{IN}$  within the working voltage range, said piecewise continuous function of  $V_{IN}$  having  $K$  pieces, wherein each two consecutive pieces of the  $K$  pieces are discontinuously joined together, wherein the relative error within each said piece of the  $K$  pieces is a monotonically decreasing function of  $V_{IN}$ , and wherein each piece of the  $K$  pieces has about a same maximum relative error.

27. The method of claim 22, wherein  $K=2$ , wherein the A/D converter apparatuses  $Z_1$  and  $Z_2$  comprise A/D converters  $B_1$  and  $B_2$  having working voltage ranges  $\delta_1$  and  $\delta_2$ , respectively, such that  $\delta_2$  is a subset of  $\delta_1$  and  $\delta_2/\delta_1$  is an integer subject to  $\delta_2/\delta_1 > 1$ , wherein  $B_1$  and  $B_2$  are respectively adapted to convert  $V_{IN}$  to  $S_1$  and  $S_2$ , and wherein said combining includes generating the digital output as essentially  $S_2$  if  $S_2$  is not within the voltage range  $\delta_1$  else said combining includes generating the digital output essentially as  $S_1$  multiplied by  $\delta_2/\delta_1$ .

28. The method of claim 27, wherein  $\delta_2/\delta_1 = 2^J$ , and wherein  $J$  is a positive integer.